REMARKS

Claims 1-9 and 26-33 remain pending in the application, with claims 1, 26 and 33 being the independent claims. Reconsideration and further examination are respectfully requested.

Initially, an objection was made to the Abstract based on its format. In response, the Abstract has been revised and is now believed to comply with all applicable requirements. Accordingly, withdrawal of this objection is respectfully requested.

In the Office Action, claims 1, 2, 3, 8 and 33 were rejected under 35 USC § 102(e) over U.S. Patent 6,526,539 (Yano); claims 26 and 32 were rejected under 35 USC § 102(e) over U.S. Patent 6,359,938 (Keevill); claims 4-7 were rejected under 35 USC § 103(a) over Yano in view of U.S. Patent 6,631,491 (Shibutani); claim 9 was rejected under 35 USC § 103(a) over Yano in view of U.S. Patent 6,014,411 (Wang); claims 27-29 were rejected under 35 USC § 103(a) over Keevill in view of U.S. Patent 4,394,753 (Penzel); and claims 30-31 were rejected under 35 USC § 103(a) over Keevill in view of Wang.

In partial response to the foregoing rejections, Applicant is submitting herewith a declaration under 37 CFR 1.131 from Applicant and a supporting declaration from Applicant's attorney. These declarations show that Applicant conceived the present invention prior to Yano's § 102(e) date of May 18, 2000, and acted with due diligence from prior to such date to the filing of the present patent application. Based on these declarations, Applicant respectfully requests withdrawal of Yano as a prior-art reference in this case and an indication that claims 1-9 and 33 (which were rejected over Yano) are now allowed.

Independent claim 26 concerns an apparatus for decoding input data. Because claim 26 comprises a number of interrelated components, solely for the purpose of facilitating an understanding of the claim, it will be discussed with reference to an exemplary embodiment, which embodiment is illustrated in Figure 3 of the present Specification.

The decoding apparatus of claim 26 includes input means (52) for inputting coded data and buffering means (88) for inputting, storing and outputting data. A first register means (96) stores a portion of the data output from the buffering means (88), and a first read/write means (94) controls writing of the data into the first register means (96) and reading of the data out of the first register means (96) so as to change the order of the data. Decoding means (82) decodes a combination of at least part of the coded data provided by the input means (52) and the data read out of the first register means (96). A second register means (84) stores data output by the decoding means (82), and a second read/write means (86) controls writing of the data into the second register means (84) and reading of the data out of the second register means (84) so as to change the order of the data, with the data read out of the second register means (84) being stored in the buffering means (88). A third register means (90) is coupled to the buffering means (88), and a third read/write means (92) transfers the data out of a portion of the buffering means (88) into the third register means (90) and then transfers the same data from the third register means (90) back into the portion of the buffering means (88), but in a different order, and then repeats the transferring steps for different portions of the buffering means (88).

The structure recited in independent claim 26 typically can provide an efficient device for decoding data using only a single decoder and a single buffer. As indicated below, various features of the apparatus recited in claim 26 are not disclosed by Keevill.

For example, the recited third read/write means, together with the recited third register means, repeatedly, for different portions of the recited buffer means, transfers the data out of the subject portion of the buffering means and then transfers the same data back into the subject portion of the buffering means, but in a different order. In this regard, the Office Action has asserted: (i) that the recited buffering means reads on Keevill's buffer 254 (shown in Figure 23 of Keevill), (ii) that the recited third register means reads on Keevill's feedback shift registers or storage registers (it is not clear which, or which element it is in Keevill's drawings) as discussed in column 7 lines 59-61 of Keevill, and (iii) that the recited third reader/write means reads on Keevill's symbol deinterleaver 182 (shown in Figure 15 of Keevill).

Just with respect to this feature of the invention, there are several problems with the assertion of anticipation over Keevill. First, as indicated in the preceding sentence, it is not clear what in Keevill the Office Action is equating with the recited third register means. Accordingly, it is not possible to know whether that element has any relationship whatsoever to Keevill's symbol deinterleaver 182 or to his buffer 254.

However, it is clear that Keevill's symbol deinterleaver 182 does not have the above-referenced relationship to his buffer 254, i.e., as is presently recited in claim 26. In this regard, Keevill's symbol deinterleaver 182 is part of his digital receiver back end shown in Figure 15, while Keevill's buffer 254 is shown in his Figure 23 and, therefore,

buffer 254 is part of his FFT and channel correction group, shown in Figure 14. See, e.g., column 18 lines 5-8 and column 9 lines 52-53 of Keevill.

As described at column 18 lines 29-59 of Keevill, data processed by Keevill's FFT and channel correction group, shown in Figure 14, are simply passed to his digital receiver back end, shown in Figure 15. There is absolutely no indication that anything at all in Keevill's digital receiver back end (much less symbol deinterleaver 182) repeatedly causes, for different portions of Keevill's buffer 254 (in his FFT and channel correction group), data to be transferred out of the subject portion of his buffer 254 and then causes the same data to be transferred back into the subject portion of buffer 254, but in a different order. Rather, it merely appears Keevill's data are processed sequentially, first in Keevill's FFT and channel correction group, shown in Figure 14, and then in his digital receiver back end, shown in Figure 15.

A careful analysis and attempt to read the various limitations of independent claim 26 on the structures asserted in the Office Action would reveal additional differences between claim 26 and such structures. However, lacking even a single feature of the present invention, such as pointed out above, is sufficient to overcome an allegation of anticipation based on Keevill's disclosure.

Specifically, the criteria for showing anticipation under § 102 have been set forth as follows:

> "For a prior art reference to anticipate in terms of 35 U.S.C. § 102, every element in the claimed invention must be shown in a single reference." [citation omitted] These elements must be arranged as in the claim under review...

In re Bond, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990).

Based on the differences between claim 26 and the applied art, claim 26 is believed to be allowable over the applied art. The other rejected claims in this application depend from claim 26, and are therefore believed to be allowable for at least the same reasons. Because each dependent claim also defines an additional aspect of the invention, however, the individual reconsideration of each on its own merits is respectfully requested.

In view of the foregoing remarks, it is believed that the entire application is in condition for allowance, and an indication to that effect is respectfully requested.

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Respectfully submitted,

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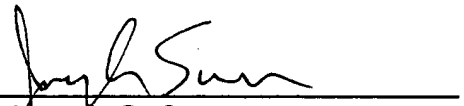
By 

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